CLAIMS

1. VLIW processor comprising:
a plurality of functional units **(1, 3, 5,** 7);

a distributed register file **(9, 11, 13, 15)** accessible by the functional units **(1, 3,** 5, 7);
and a partially connected communication network (17) for coupling the functional units **(1, 3, 5,** 7) and selected parts of the distributed register file **(9, 11, 13, 15);** characterized in that the VLIW processor further comprises communication means (29) for coupling the functional units **(1, 3, 5,** 7) and the distributed register file **(9, 11, 13, 15).**

2. A VLIW processor according to Claim 1 wherein:
the communication means (29) comprise a multiplexer (31) and a bus (33), the multiplexer (31) being arranged for coupling the functional units **(1, 3, 5,** 7) and the bus (33), the bus (33) being arranged for coupling the multiplexer (31) and the distributed register file **(9, 11, 13, 15).**

3. A VLIW processor according to Claim 1 wherein:
the communication means (29) are arranged for communication with a first latency, the partially connected communication network (17) is arranged for communication with a second latency, the first latency exceeding the second latency.

4. A VLIW processor according to Claim 2 wherein: the
bus (33) comprises at least one pipeline register (35).

5. A VLIW processor according to Claim 2 wherein:
the multiplexer (31) comprises at least one register.

6. A VLIW processor according to Claim 1, comprising a first plurality **(101)** of functional units **(105, 107)** and a second plurality **(103)** of functional units **(109, 111, 113);**

a first pass unit (171) associated with one (107) of the functional units (105, 107) of the first plurality **(101)** for passing data from one **(121)** of the distributed register files **(115, 117, 119, 121)** associated with the first plurality (101) of functional units to one of the distributed register files **(123, 125, 127, 129, 131, 133)** associated with the second plurality **(103)** of functional units **(109, 111, 113);**

and a second pass unit (173) associated with one (113) of the functional units **(109, 111, 113)** of the second plurality (103) for passing data from one (133) of the distributed register files **(123, 125, 127, 129, 131, 133)** associated with the second plurality (103) of functional units to one of the distributed register files **(115, 117, 119, 121)** associated with the first plurality (101) of functional units **(105, 107);**

7. A VLIW processor according to Claim 6 wherein:
the pass units (171, 173) are part of the respectively associated functional units **(107, 113).**

8. A VLIW processor according to Claim 1 wherein:
the communication means (29) couple the functional units **(1, 3, 5,** 7) and all parts of the distributed register file **(9, 11, 13, 15).**